Display control
This module reads screen data from the External RAMs (D1204 and D1205) and sends it to the LCD. It also sends line pulses LINECL (17 kHz) and frame pulses FRAME (70 Hz). This screen data, consisting of for example cursor and grid information, is stored in External RAMs as bitplane information. The trace data is stored as a value for every vertical line on the LCD. This data is converted to bitplane data and added to the cursor and grid information. The display control module also makes it possible to change the dotsize of the signal displayed and to use dot joining.

Decoding and synchronization (DESY)
The DESY section is the decoder for the D-ASIC's internal addresses. This module also synchronises the microprocessor with the D-ASIC's Display control module, as both access the same Acquisition RAM.

Digital to analog converters (DACs)
The DACs module contains 10 one-bit pulse width modulated monotonous DACs, whose resolution ranges from five to ten bits. The DACs are used to control level shifting, analog trigger level, LCD contrast and the generator function (see section 3.4.7).

External RAMs

The External RAM section consists of two 32K * 8 SRAMs (D1204 and D1206). These RAMs contain:

- waveforms (stored with the WAVEFORM key)
- frontsettings (stored with the SETUP key)
- bitplane data for the LCD picture
- text, to be used on the display
- data in RECORD mode
- data in A versus B mode (A= ↑ B= →)
- bitplane data used while making a printout of the screen

Ram Power circuit
The External RAMs are powered by the RAM Power circuit. The RAM Power circuit is fed directly by the batteries, independently of the main power supply.
The RAM Power circuit is a simple oscillator, used to generate a stabilised voltage +VRAM out of the battery voltage -VBAT. The basic oscillator circuit is shown in figure 3.5.

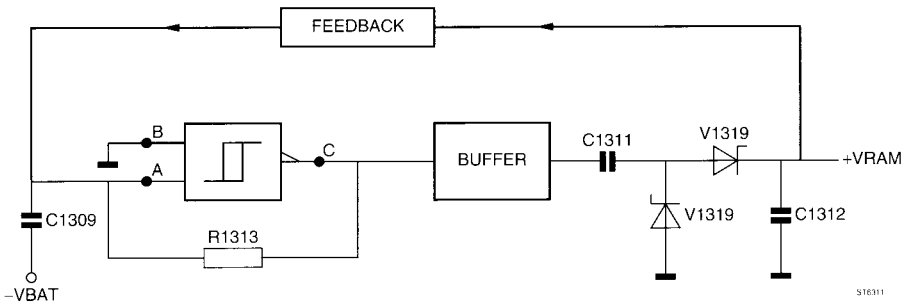

Figure 3.5 Oscillator RAM Power circuit

Input B of Schmitt input NAND D1301 is connected to ground. When the voltage on input A is also "low", the output C will become "high". Capacitor C1309 will charge via R1313. After some time input A will become "high", resulting in a "low" output C.

Capacitor C1309 will then discharge via resistor R1313. The generated output pulses are buffered and converted into a DC voltage by C1311, C1312 and V1319. The output voltage +VRAM is fed back to the NAND input A, via several transistors (voltage gap). If the output voltage +VRAM has reached the correct value, the pulse train at NAND output C is stopped via this feedback (see figure 3.6). In